

WHAT IS CLAIMED IS:

1 1. A digital embedded architecture, including a microcontroller and a memory
2 device, suitable for reconfigurable computing in digital signal processing and
3 comprising: a processor, structured to implement a Very Long Instruction Word
4 elaboration mode by a general purpose hardwired computational logic, and an
5 additional data elaboration channel comprising a reconfigurable function unit based
6 on a pipelined array of configurable look-up table based cells controlled by a special
7 purpose control unit.

1 2. A digital embedded architecture according to claim 1, wherein said
2 reconfigurable function unit includes a hardware-based Field Programmable Gate
3 Array (FPGA) embedded devices.

1 3. A digital embedded architecture according to claim 1, wherein said additional
2 data elaboration channel is tightly integrated in a processor core, receiving inputs
3 from a register file and writing results on dedicated write back channels over the
4 register file.

1 4. A digital embedded architecture according to claim 1, wherein said pipelined
2 array of configurable lookup-table based cells implements a configurable run-time
3 with a variable latency data path capable to emulate a potentially infinite number of
4 virtual application specific function units.

1 5. A digital embedded architecture according to claim 4, wherein the architecture
2 is based on three different and concurrent data elaboration flows, two of which feed
3 each cycle by instruction fetch and one based on an independent, variable latency
4 pipeline implemented on the configurable data-path.

1 6. A digital embedded architecture according to claim 2, wherein said
2 configurable gate-array is a Pipelined-Configurable-Array (PiCo-Array) comprising a
3 pipelined array of configurable lookup-table based cells virtually emulating a
4 microprocessor data path.

1 7. A digital embedded architecture according to claim 6, wherein the cells of said
2 PiCo-Array structure are grouped in rows, each representing a possible stage of a
3 customized pipeline, and the whole array can be represented by a control data flow
4 graph, each row or group of rows corresponding to a different state.

1 8. A digital embedded architecture according to claim 3, wherein at any decoded
2 instruction of the pipelined array a corresponding destination register file is locked,
3 so that any following instruction trying to access such a register will cause a
4 processor stall; normal execution being restored only when the pipelined array
5 completes the write-back operation unlocking its destination register.

1 9. A digital embedded architecture according to claim 3, wherein said special
2 purpose control unit is a hardwired, run-time programmable Data-Flow-Graph based
3 control unit synchronizing the pipelined computation of the gate-array cells.

1 10. A digital embedded architecture according to claim 8, wherein the locking
2 mechanism of said register file supports the highest possible level of resource
3 utilization parallelism allowing unpredictable latency instructions to be executed on
4 the configurable unit without altering program flow consistency.

1 11. A digital embedded architecture according to claim 3, wherein said register file
2 comprises four read ports, used to support the issue of two RISC instructions each
3 clock cycle, and two write ports reserved for said two hardwired pipeline channels;
4 two other ports being entirely dedicated to write back results of the pipelined array,
5 thus avoiding introduction of dedicated logic handling competition on the register file
6 ports.

1 12. A digital embedded architecture according to claim 1, wherein said pipelined
2 array comprises a first level cache, storing four configurations for each logic cell; and
3 further comprising a context switch for taking only one clock cycle and providing four
4 immediately available instructions.

1 13. A digital embedded architecture according to claim 1, further comprising a
2 specific extension of the instruction set architecture for controlling configuration and

3 execution over the configurable array, said instruction set architecture including 32-
4 bit and 64-bit instructions taking advantage of the entire VLIW instruction word.

1 14. A digital embedded architecture according to claim 1, further comprising a
2 special purpose reconfiguration mechanism for allowing very fast configuration
3 completely concurrent with processor execution, said reconfiguration mechanism
4 including the configurable array being structured in blocks, having at least eight rows
5 each, each block being reprogrammed while the other blocks are under execution.

1 15. A circuit, comprising:
2 a processor configured to implement a plurality of concurrent data elaboration
3 flows;
4 a programmable logic device coupled to the processor and performing a data
5 elaboration function; and
6 a control device coupled to the logic device and controlling operation of the
7 logic device.

1 16. The circuit of claim 15, wherein the logic device comprises a hardware-based
2 Field Programmable Gate Array.

1 17. The circuit of claim 15, wherein the logic device comprises a pipelined array of
2 configurable lookup-table based cells emulating a microprocessor data path.

1 18. The circuit of claim 15, wherein the logic device implements a configurable
2 run-time with a variable latency data path.

1 19. The circuit of claim 17, wherein the control device synchronizes the pipelined
2 computation of the gate-array cells.

1 20. A computer system, comprising:
2 a memory device; and
3 a semiconductor chip, comprising:
4 a processor configured to implement a plurality of concurrent data
5 elaboration flows;

6 a programmable logic device coupled to the processor and performing
7 a data elaboration function; and
8 a control device coupled to the logic device and controlling operation of
9 the logic device.

1 21. A method of algorithmic data elaboration, comprising:
2 employing a processor to elaborate a first portion of the algorithmic data;
3 employing a programmable logic device coupled to the processor to elaborate
4 a second portion of the algorithmic data, operation of the logic device being
5 controlled by a control device.

1 22. The method of claim 21, wherein the logic device comprises a pipelined array
2 of configurable lookup-table based cells emulating a microprocessor data path.

1 23. The method of claim 21, wherein:
2 employing a processor comprises writing data to a register file over a first port
3 dedicated to the processor; and
4 employing a programmable logic device comprises writing data to the register
5 file over a second port dedicated to the logic device.

1 24. The method of claim 23, wherein employing a programmable logic device
2 further comprises:
3 decoding a logic device instruction; and
4 locking a destination register of the register file in response to decoding the
5 logic device instruction, the destination register corresponding to the instruction.

1 25. The method of claim 24, wherein employing a programmable logic device
2 further comprises unlocking the destination register in response to writing data to the
3 register file over the second port.